CLAIMS

What is claimed is:

1. A method for testing circuits having analog components, comprising:

performing a low-cost optimized test on the circuit by applying an optimized input stimulus to the circuit;

capturing the circuit response to the input stimulus applied to the circuit;

evaluating the circuit response to predict whether the performance parameters of the circuit satisfies predetermined specifications for the circuit; and

making a pass/fail determination for the circuit based upon the evaluation of the circuit response.

2. The method of claim 1, wherein the low-cost optimized test is used to evaluate compliance with each specification specified for the circuit being tested.

3. The method of claim 1, wherein the low-cost optimized test is used to evaluate compliance with less than each specification specified for the circuit being tested.

4. The method of claim 1, wherein the low-cost optimized test is designed to maximize the sensitivity of the circuit response to changes in circuit process parameters.

5. The method of claim 1, further comprising performing specification based tests to circuits for which a clear pass/fail determination could not be made from the low-cost optimized test.

6. The method of claim 5, wherein the specification based tests are applied to determine compliance with respect to less than all of the specification for the circuit being tested.

7. The method of claim 5, wherein the optimized test is created such that the number of specification based tests needed is minimized.

8. The method of claim 1, further comprising performing specification based tests to the circuits to determine compliance with one or more predetermined circuit specifications.

9. The method of claim 8, wherein the specification based tests are applied to less than all of the specifications specified for the circuit being tested.

10. The method of claim 1, wherein the low-cost optimized test is formulated by deriving synthesizing functions which map the measurement response to circuit performance parameters.

11. The method of claim 10, wherein one synthesizing function is derived for each circuit specification to be tested.

12. The method of claim 10, wherein the circuit response is input into the synthesizing functions to predict compliance with the various circuit specifications.

13. The method of claim 10, wherein the synthesizing functions are derived near the boundary of an acceptance boundary for each circuit performance parameter.

14. The method of claim 10, wherein the synthesizing functions are derived through nonlinear regression.

15. The method of claim 1, wherein the input stimulus is a sinusoidal stimulus.

16. The method of claim 1, wherein the input stimulus is derived using genetic algorithms.

17. A method for testing circuits having analog components, comprising:

deriving synthesizing functions which map measurement responses of the circuit to circuit performance parameters;

applying an optimized input stimulus to the circuit;

capturing the circuit response to the input stimulus applied to the circuit;

evaluating the circuit response with respect to the derived synthesizing functions to predict whether a predetermined number of performance parameters of the circuit satisfies predetermined specifications for the circuit;

making a pass/fail determination for the circuit based upon the evaluation of the circuit response; and

for circuits for which a clear pass/fail determination cannot be made, performing specification based tests with respect to particular predetermined circuit specifications to make a final pass/fail determination for the circuit.

18. The method of claim 17, wherein the low-cost optimized test is designed to maximize the sensitivity of the circuit response to changes in circuit process parameters.

19. The method of claim 17, wherein the optimized test is created such that the number of specification based tests needed is minimized.

20. The method of claim 17, wherein one synthesizing function is derived for

each circuit specification to be tested.

21. The method of claim 17, wherein the synthesizing functions are derived near the boundary of an acceptance boundary for each circuit performance parameter.

22. The method of claim 17, wherein the input stimulus is derived using genetic algorithms.

23. A testing system for testing compliance of circuits with predetermined circuit specifications, comprising:

logic configured to derive an optimized input stimulus which is to be applied to the circuit being tested;

logic configured to derive synthesizing functions which map measurement responses of the circuit to circuit performance parameters;

logic configured to capture the circuit response to the input stimulus applied to the circuit; and

logic configured to evaluate the circuit response through use of the derived synthesizing functions to predict whether the performance parameters of the circuit satisfies the predetermined specifications for the circuit.

24. The system of claim 23, wherein the derived synthesizing functions are designed to maximize the sensitivity of the circuit response to changes in circuit process parameters.

25. The system of claim 23, wherein the synthesizing functions are derived near the boundary of an acceptance boundary for each circuit performance parameter.

26. A testing system for testing compliance of circuits with predetermined circuit specifications, comprising:

means for deriving an optimized input stimulus which can be applied to the circuit being tested;

means for deriving synthesizing functions which map measurement responses of the circuit to circuit performance parameters;

means for capturing the circuit response to the input stimulus applied to the circuit; and

means for evaluating the circuit response through use of the derived synthesizing functions to predict whether the performance parameters of the circuit satisfies the predetermined specifications for the circuit.

27. The system of claim 26, wherein the derived synthesizing functions are designed to maximize the sensitivity of the circuit response to changes in circuit process parameters.

28. The system of claim 26, wherein the synthesizing functions are derived near the boundary of an acceptance boundary for each circuit performance parameter.